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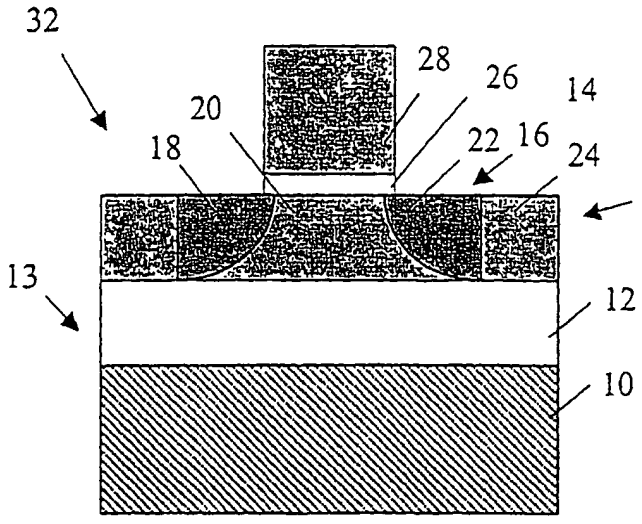

(57) Abstract: A semiconductor device, such as a memory device or radiation detector, is disclosed, in which data storage cells are formed on a substrate 13. Each of the data storage cells includes a field effect transistor having a source 18, drain 22 and gate 28, and a body arranged between the source and drain for storing electrical charge generated in the body. The magnitude of the net electrical charge in the body 22 can be adjusted by input signals applied to the transistor, and the adjustment of the net electrical charge by the input signals can be at least partially cancelled by applying electrical voltage signals between the gate 28 and the drain 22 and between the source 18 and the drain 22.

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SEMICONDUCTOR DEVICE

The present invention relates to semiconductor devices, and relates particularly, but not exclusively, to DRAM memory devices using SOI (silicon on insulator) technology.

DRAM memories are known in which each memory cell consists of a single transistor and a single capacitor, the binary 1's and 0's of data stored in the DRAM being represented by the capacitor of each cell being in a charged or discharged state. Charging and discharging of the capacitors is controlled by switching of the corresponding transistor, which also controls reading of the data stored in the cell. Such an arrangement is disclosed in US patent 3387286 and will be familiar to persons skilled in the art.

Semiconductor devices incorporating MOSFET (metal oxide semiconductor field effect transistor) type devices are well known, and arrangements employing SOI (silicon on insulator) are becoming increasing available. SOI technology involves the provision of a silicon substrate carrying an insulating silicon dioxide layer coated with a layer of silicon in which the individual field effect transistors are formed by forming source and drain regions of doped silicon of one polarity separated by a body of doped silicon of the opposite polarity.

SOI technology suffers the drawback that because the body region of each individual transistor is electrically insulated from the underlying silicon substrate, electrical charging of the body can occur under certain conditions. This can have an effect on the electrical performance of the transistors and is

generally regarded as an undesirable effect. Extensive measures are generally taken to avoid the occurrence of this effect, as described in more detail in a suppression of parasitic bipolar action in ultra thin film fully depleted CMOS/simox devices by Ar-ion implantation into source/drain regions@ published by Terukazu Ohno et al in IEEE Transactions on Electron Devices, Vol 45, Number 5, May 1998.

A known DRAM device is also described in US patent 4298962, in which the DRAM is formed from a plurality of cells, each of which consists of an IGFET (insulated gate field effect transistor) transistor formed directly on a silicon substrate. This DRAM enables the injection of charge carriers from a semiconductor impurity region of opposite polarity to the polarity of the source and drain regions and which is located in the source or drain, or the injection of charge carriers from the silicon substrate.

This known device suffers from the drawback that it requires at least four terminal connections for its operation (connected to the drain, gate, source and impurity region of opposite polarity or to the substrate), which increases the complexity of the device. Furthermore, the memory function of each cell is ensured only while voltages are being applied to the transistor source and drain, which affects the reliability of the device, and writing, reading and refreshing of the stored information must be performed in so-called Apunch through@ mode, which results in heavy power consumption by the device.

An attempt to manufacture DRAM memories using SOI technology is disclosed in US patent 5448513. In that known device, each

memory cell is formed from two transistors, one of which is used for writing data to the memory cell, and one of which is used for reading data stored in the device. As a result of each cell consisting of two separate transistors, each cell requires four terminal connections for its operation, which increases the complexity of the device, as well as the surface area necessary for each memory cell as a result of the provision of two transistors.

Preferred embodiments of the present invention seek to overcome the above disadvantages of the prior art.

According to an aspect of the present invention, there is provided a semiconductor device comprising :-

a substrate;

at least one data storage cell provided on one side of said substrate, wherein the or each said data storage cell comprises a respective field effect transistor comprising (i) a source; (ii) a drain; (iii) a body arranged between said source and said drain and adapted to at least temporarily retain a net electrical charge generated in said body such that the magnitude of said net charge can be adjusted by input signals applied to said transistor; and (iv) at least one gate adjacent said body; and

charge adjusting means for at least partially cancelling the adjustment of said net electrical charge by said input signals, by applying first predetermined electrical voltage signals between at least one corresponding said gate and the

corresponding said drain and between the corresponding said source and said drain.

The present invention is based upon the surprising discovery that the previously undesirable characteristic of excess electrical charge generated and retained in the body of the transistor can be used to represent data. By providing a semiconductor device in which data is stored as an electrical charge in the body of a field effect transistor, this provides the advantage that a much higher level of circuit integration is possible than in the prior art, since each data cell, for example when the semiconductor device is a DRAM memory, no longer requires a capacitor and can consist of a single transistor. Furthermore, by generating said electrical charge in the body of the field effect transistor (as opposed to in the substrate or in an impurity region provided in the source or drain), this provides the further advantage that no specific connection need be made to the substrate or impurity region, thus reducing the number of terminal connections necessary to operate the device.

In a preferred embodiment, said input signals comprise second predetermined electrical voltage signals applied between at least one corresponding said gate and the corresponding said drain and between the corresponding said source and said drain.

The device may be a memory device.

The device may be a sensor and the charge stored in at least one said body in use represents a physical parameter.

The input signals comprise electromagnetic radiation.

The device may be an electromagnetic radiation sensor.

The device may further comprise a first insulating layer at least partially covering said substrate, wherein the or each said data storage cell is provided on a side of said first insulating layer remote from said substrate.

The first insulating layer may comprise a layer of semiconductor material of opposite doping type to the body of the or each said data storage cell.

By providing a layer of material of opposite doping type to the transistor body (e.g. a layer of n-type material in the case of a p-type transistor body), this provides the advantage that by suitable biasing of the insulating layer such that the body/ insulating layer junction is reverse biased, adjacent transistors can be electrically isolated from each other without the necessity of using silicon-on-insulator (SOI) technology in which a layer of dielectric material such as silicon oxide is formed on a silicon substrate. This in turn provides the advantage that devices according to the invention can be manufactured using conventional manufacturing techniques.

The device may further comprise a respective second Insulating layer provided between at least one said body and the or each corresponding said gate.

In a preferred embodiment, at least one said transistor includes a plurality of defects in the vicinity of the interface between at least one corresponding said body and the corresponding said second insulating layer, for trapping charge carriers of opposite polarity to the charge carriers stored in the body.

This provides the advantage of enabling the charge stored in the body of the transistor to be reduced by means of recombination of the stored charge carriers with charge carriers of opposite polarity trapped in the vicinity of the interface.

The density of defects in the vicinity of said interface may be between 10^9 and 10^{12} per cm^2.

The device may further comprise data reading means for causing an electrical current to flow between a said source and a said drain of at least one said data storage cell by applying third predetermined electrical voltage signals between at least one corresponding said gate and said drain and between said source and said drain.

The first insulating layer may comprise a plurality of insulating layers.

At least one said data storage cell may be adapted to store at least two distinguishable levels of said electrical charge.

In a preferred embodiment, at least one said data storage cell is adapted to store at least three distinguishable levels of said electrical charge.

This provides the advantage that the more distinguishable charge levels there are which can be used to represent data in a data storage cell, the more bits of data can be stored in each cell. For example, in order to represent n bits of data, 2^n distinguishable charge levels are required, as a result of which high density data storage devices can be created.

At least one said transistor may have a drain/body capacitance greater than the corresponding source/body capacitance.

This provides the advantage of reducing the voltages which need to be applied to the transistor to adjust the charge stored in the body thereof, which in turn improves reliability of operation of the device.

The body of at least one said transistor may have a higher dopant density in the vicinity of said drain than in the vicinity of said source.

The area of the interface between the drain and body of at least one said transistor may be larger than the area of the interface between the source and the body.

Common source and/or drain regions may be shared between

adjacent transistors of said device.

This provides the advantage of improving the extent to which the device can be miniaturised.

According to another aspect of the present invention, there is provided a method of storing data in a semiconductor device comprising a substrate, and at least one data storage cell provided on one side of said substrate, wherein the or each said data storage cell comprises a respective field effect transistor comprising (i) a source; (ii) a drain; (iii) a body arranged between said source and said drain and adapted to at least temporarily retain a net electrical charge generated in said body such that the magnitude of said net charge can be adjusted by input signals applied to said transistor; and (iv) at least one gate adjacent said body; the method comprising the steps of:

applying first predetermined electrical voltage signals between at least one corresponding said gate and the corresponding said drain and between the corresponding said source and said drain to at least partially cancel the adjustment of said net charge by said input signals.

The method may further comprise the step of applying second predetermined electrical voltage signals between at least one said gate of a said data storage cell and the corresponding said drain and between the corresponding said source and said drain.

The step of applying second predetermined said electrical

signals may adjust the charge retained in the corresponding said body by means of the tunnel effect.

This provides the advantage of enabling the charge adjustment to be carried out in a non-conducting state of the transistor in which the only current is the removal of minority charge carriers from the body of the transistor. This in turn enables the charge adjustment operation to involve very low power consumption. This also provides the advantage that a considerably higher charge can be stored in the body of the transistor since, it is believed, the charge is stored throughout substantially the entire body of the transistor, as opposed to just that part of the transistor in the vicinity of the first insulating layer. As a result, several levels of charge can be stored, representing several bits of data.

The charge may be adjusted by the application of a voltage signal between at least one said gate and the corresponding drain such that at the interface between the corresponding body and the drain, the valence and conduction bands of the body and drain are deformed to inject electrons from the valence band to the conduction band by the tunnel effect, causing the formation of majority carriers in the body.

Said charge may be adjusted by means of tunnelling of electrons from the valence band to at least one gate of a said field effect transistor.

The step of applying first predetermined said voltage signals may comprise applying electrical voltage signals between at least one said gate and the corresponding said drain such that

at least some of the charge carriers stored in the corresponding body recombine with charge carriers of opposite polarity in said body.

This provides the advantage that the charge stored in the particular transistor body can be adjusted without the transistor being switched into a conductive state, as a result of which the charge adjustment can be carried out at very low power consumption. This feature is especially advantageous in the case of a semiconductor device incorporating a large number of transistors, such as an optical detector in which individual pixels are provided by transistors.

The process, operating under the principle known as charge pumping, and described in more detail in the article by G Groeseneken et al AA reliable approach to charge pumping measurements in MOS transistors@, IEEE Transactions on Electron Devices, Vol 31, pp 42 to 53, 1984 provides the advantage that it operates at very low current levels, which enables power consumption in devices operating according to the process to be minimised.

The method may further comprise the step of applying at least one said voltage signal comprising a first part which causes a conducting channel to be formed between the source and the drain, the channel containing charge carriers of opposite polarity to the charge carriers stored in said body, and a second part which inhibits formation of the channel, and causes at least some of said stored charge carriers to migrate towards the position previously occupied by said channel and recombine with charge carriers of opposite polarity previously in said

channel.

The method may further comprise the step of repeating the step of applying at least one said voltage signal in a single charge adjustment operation sufficiently rapidly to cause at least some of said charge carriers stored in the body to recombine with charge carriers of opposite polarity before said charge carriers of opposite polarity can completely migrate to said source or said drain.

Preferred embodiments of the invention will now be described, by way of example only and not in any limitative sense, with reference to the accompanying drawings, in which:-

Figure 1 is a schematic representation of a first embodiments of a MOSFET type SOI transistor for use in a semiconductor device embodying the present invention;

Figure 2 shows a sequence of electrical pulses to be applied to the transistor of Figure 1 to generate a positive charge in the body of the transistor according to a first method;

Figure 3 shows a sequence of electrical pulses to be applied to the transistor of Figure 1 to generate a negative charge in the body of the transistor according to a first method;

Figure 4 shows the variation in source-drain current of the transistor of Figure 1 as a function of gate voltage, with the body of the transistor being positively charged, uncharged and negatively charged;

Figure 5a is a schematic representation of an SOI MOSFET transistor of a second embodiment for use in a semiconductor device embodying the present invention;

Figure 5b is a representation of the effect of the application of a gate voltage to the transistor of Figure 5a on the valence and conduction bands of the transistor;

Figures 6a to 6c illustrate a first method embodying the present invention of eliminating a positive charge stored in the body of the transistor of Figure 1;

Figures 7a to 7d illustrate a second method embodying the present invention of eliminating a positive charge stored in the body of the transistor of Figure 1;

Figure 8 is a schematic representation of a SOI MOSFET transistor of a third embodiment for use in a semiconductor device embodying the present invention;

Figure 9 is a schematic representation of the gate, source and drain areas of a transistor of a fourth embodiment for use in a semiconductor device embodying the present invention;

Figures 10 and 11 show multiple charging levels of the transistor of Figure 1;

Figure 12 shows multiple charging levels of the transistor of Figure 1 achieved by means of the methods of Figures 6 and 7;

Figure 13 is a schematic representation of part of a DRAM

memory device embodying the present invention and incorporating the transistor Figure 1, 5, 6, 7, 8 or 9;

Figure 14 is a schematic representation of part of a DRAM memory device of a further embodiment of the present invention and incorporating the transistor Figure 1, 5, 6, 7, 8 or 9;

Figure 15 is a plan view of the part of the DRAM memory device of Figure 14;

Figure 16 is a cross-sectional view along the line A-A in Figure 15;

Figure 17 shows the development of integrated circuit processor performance compared with DRAM performance; and

Figure 18 is a schematic representation of an optical sensor embodying the present invention and incorporating the transistor of Figure 1, 5, 6, 7, 8 or 9.

Referring firstly to Figure 1, an NMOS SOI (silicon on insulator) MOSFET (metal-oxide-silicon field effect transistor) comprises a silicon wafer 10 coated with a layer 12 of silicon dioxide, the wafer 10 and layer 12 constituting a substrate 13. A layer 14 formed on the substrate 13 consists of an island 16 of silicon doped with impurities to form a source 18 on n-type material, a body 20 of p-type material and a drain 22 of n-type material, together with a honeycomb insulating structure 24 of silicon dioxide, the honeycomb structure being filled by a plurality of islands 16. The source 18 and drain 22 extend through the entire thickness of the silicon layer 14. An

insulating film 26 is formed over body 20, and a gate 28 of doped semiconductor material is provided on dielectric film 26. The production process steps, chemical compositions and doping conditions used in manufacturing the transistor of Figure 1 will be familiar to persons skilled in the art, and are also described in further detail in ASOI: Materials to Systems@ by A J Auberton-Hervé, IEDM 96. This publication also discloses that transistors of this type have an electrical instability as a result of the fact that the body 20 is electrically floating, and can therefore acquire an electrical charge, depending upon the sequence of voltage pulses applied to the transistor.

The transistor shown in Figure 1 is of the type known to persons skilled in the art as "partially depleted" (PD), in which the depletion regions (i.e. those regions forming junctions between semiconductor types of opposite polarity and which are depleted of free charge carriers) do not occupy the entire thickness of the silicon layer 14.

Referring now to Figure 2, in order to generate a positive charge in the body of the NMOS transistor of Figure 1, the gate voltage V_g and drain voltage V_d, as well as the source voltage, are initially zero. At time t_0, the gate voltage is brought to -1.5V and at time $t_0 + \Delta t_0$ (where Δt_0 can be greater than, less than or equal to zero), the drain voltage V_d is brought to -2V, while the source voltage remains at zero. By applying a negative voltage pulse to the gate and a more negative voltage pulse to the drain, a concentration of negative charge forms in the body 20 in the vicinity of the gate 28, while a concentration of positive charge forms in the body in the vicinity of insulating layer 12. At the same time, a conduction

channel linking the source 18 and drain 22 forms in the body 20, allowing conduction of electrons between the source 18 and drain 22. This allows electrons to be attracted into the channel from the source 18 and/or drain 22.

The application of a negative voltage to the drain 22 relative to the source as shown in Figure 2 generates electron-hole pairs by impact ionisation in the vicinity of the source. The holes accumulated in the floating body create a positive charge.

The drain voltage V_d then returns at time t_1 to zero, and the gate voltage V_g returns to zero at $t_1 + \Delta t_1$ to remove the conductive channel between the source 18 and drain 22, the time interval $t_1 - t_0$ typically being between a few nanoseconds and several tens of nanoseconds, while Δt_1 is of the order of 1 nanosecond. It is also possible to create a positive charge in the body 20 by applying a positive drain voltage pulse, depending upon the voltages of the source, drain and gate relative to each other. It has been found in practice that in order to create a positive charge in the body, the drain voltage must be switched back to zero before the gate voltage.

Referring now to Figure 3, a negative charge is generated in the body 20 by increasing the gate voltage V_g to +1Vat t_0 while the source and drain voltages are held at zero, then reducing the drain voltage V_d to -2V at time $t_0 + \Delta t_0$ while the source voltage is held at zero. The gate voltage V_g and drain voltage V_d are then subsequently brought to zero at times t_1 and $t_1 + \Delta t_1$ respectively, where Δt_1 can be positive or negative (or zero). The application of a positive voltage to the gate 28

relative to the voltages applied to the source 18 and drain 22 again causes the formation of a conductive channel between the source 18 and drain 22, as was the case with the formation of an excess positive charge as described above with reference to Figure 2. The positive voltage applied to the gate 28 also creates a concentration of negative charge in the body 20 in the vicinity of the gate 28, and a concentration of positive charge in that part of the body remote from the gate 28, i.e. adjacent the insulating layer 12.

As a result of the application of the negative voltage to the drain 22, the body-drain junction is forward biased, as a result of which holes are conducted out of the body 20 to the drain 22. The effect of this is to create an excess of negative charge in the body 20. It should be noted that under these bias conditions the generation of holes by impact ionisation is fairly weak. Alternatively, a positive voltage pulse can be applied to the drain and the gate, as a result of which the body-source junction is forward biased and the holes are removed from the body to the source. In a similar way, instead of generating a negative charge in the body 20, a positive charge stored in the body can be removed.

Referring now to Figure 4, the drain current I_d is dependent upon the applied gate voltage V_g, and the Figure shows this relationship for a drain voltage V_d of 0.3V, the curves 34, 36 and 38 representing the body 20 having an excess of positive or negative charge, or zero excess charge respectively. It will therefore be appreciated that by the application of calibrated voltages to gate 28 and drain 22 and by measuring drain current I_d, it is possible to determine whether body 20

is positively or negatively charged, or whether it is uncharged. This phenomenon enables the transistor of Figure 1 to be used as a data storage cell, different charging levels representing data Ahigh@ and Alow@ states, or some physical parameter to be measured, as will be described in greater detail below.

Referring to Figure 5a, in which parts common to the embodiment of Figure 1 are denoted by like reference numerals but increased by 100, a further embodiment of an SOI transistor is shown in which the transistor is caused to store a positive charge in its body 120 by means of the tunnel effect. The transistor of Figure 5a is manufactured by a succession of photo lithographic, doping and etching operations which will be familiar to persons skilled in the art. The transistor is made to 0.13 μm technology with a p-type dopant density of 10^{18} atoms per cm^3 in the body 120 and of 10^{21} n-type atoms per cm^3 in the drain 122. The insulating layer 126 has a thickness of the order of 2nm.

In order to operate the transistor of Figure 5a, the source is held at 0V, the gate voltage V_g is -1.5V and the drain voltage V_d is + 1V. This causes the tunnel effect at the interface of the body 120 and drain 122 as a result of the fact that the valence band B_v and conduction band B_c, represented schematically in Figure 5b, are distorted. Folding of these bands can be achieved by an electric field of the order of 1MV/cm, which results in electrons being extracted by the drain 122, while the associated holes remain in the body 120. This physical phenomenon is known as AGIDL@ (Gate Induced Drain Leakage), described in greater detail for example in the

article by Chi Chang et al ACorner Field Induced Drain Leakage in Thin Oxide MOSFETS@, IEDM Technical Digest, Page 714, 1987.

The charging operation of Figure 5a has the advantage over that described with reference to Figures 1 to 3 that the only current flowing during the charging process is the extraction of electrons from the body 120 by the tunnel effect. As a result, charging occurs at very low power consumption. Furthermore, it has been found that the charge which can be stored in the body 120 is considerably higher (approximately twice as large) than that obtained by previous methods. It is believed that this is as a result of the fact that a charge is stored throughout the entire volume of the body 120, not just in that part of the body 120 adjacent to the insulating layer 112.

It will be appreciated by persons skilled in the art that the process of Figure 5a, which was described with reference to NMOS transistors, can also be applied to PMOS transistors, in which case the gate voltage is positive and the drain voltage negative, and holes are extracted by the drain while electrons are trapped.

Referring now to Figures 6a to 6c, in which parts common to the embodiment of Figure 1 are denoted by like reference numerals but increased by 200, a process is described for removing charge stored in the body 220 of the transistor. It is important that the body 220 of the transistor and the insulating film 226 be separated by an interface 230 a few atomic layers thick which provides defects forming sites to which electrons can attach.

In order to remove the charge stored in the body 220, a cyclical signal shown in the upper part of Figure 6a is applied to the gate, the instant illustrated by Figure 6a being shown by an arrow in the insert. Initially, a potential of 0V is applied to the source 218 and drain 222, and then a potential of 0.8V is applied to gate 228. This has the effect of creating a conducting channel 232 at interface 230, and electrons are attracted into the channel 232 from the source 218 and/or drain 222. The channel 232 has a high density of electrons 234, as a result of the positive voltage applied to gate 228, of which some are attached to defects at the interface 230.

When a voltage of -2.0V is then applied to gate 228, as indicated Figure 6b, the channel 232 disappears, but the bound electrons 234 remain in the interface 230. Moreover, the voltage applied to the gate 228 tends to cause holes 236 to migrate towards the interface 230 where they recombine with the bound electrons 234. As can be seen in Figure 6c, when a further cycle is applied beginning with the application of a voltage of 0.8V to gate 228, the channel 232 is again formed. However, compared to the situation illustrated in Figure 6a, the number of holes 236 has decreased.

The interface 230 preferably has a defect density between 10^9 and 10^{12} per cm^2, this density and the number of oscillations necessary to remove the particles forming the stored charge representing an acceptable compromise between device performance being limited by the number of defects and assisted by the number of trapped electrons. The pulse duration is typically about 10ns, the rise and falling time being of the

order of 1ns. It should also be noted that in certain types of transistor, it is also possible to form a channel between the source 218 and the drain 222 in the vicinity of the insulating layer 212. In such a case, the conditions for recombination of charge carriers are slightly different, but the principle of operation is generally the same.

Figure 7a shows a transistor identical in construction to that of Figures 6a to 6c, but which enables the stored charge to be reduced more rapidly than in the case of Figures 6a to 6c using recombination of charges at the interface 230, but without having electrons bound to defects. Figure 7a shows the state of the transistor before the charge reduction process is commenced, the body 220 having an excess of holes 236. By applying a positive voltage, for example 0.8V, to gate 228 as shown in Figure 7b, while keeping the source and drain at 0V, a channel 232 at the interface 230 is created. The channel 232 contains an excess of electrons 234, depending on the positive voltage applied to the gate 228, the quantity of free electrons 234 significantly exceeding that of the holes 236 present in the body 220 because of attraction of electrons into the channel 232 from the source 218 and/or drain 222.

It can be shown that by rapidly reversing the polarity of the signal applied to the gate 228, for example from 0.8V to -2.0V in a time of the order of a picosecond, the electrons 234 located in the channel 232 do not have time to migrate before the holes 236 contained in the body 220 arrive in the space previously occupied by the channel 232, as shown in Figure 7c. The holes 236 and electrons 234 recombine in the interior of the body 220 without current flowing between the source and the

drain, while the excess electrons 234 migrate towards the source 218 and the drain 222. In this way, after a very short period of time, all of the holes 236 of the stored charge are recombined, as shown in Figure 7d.

In order to achieve the switching speeds necessary for the above process to be utilised in a semiconductor device, it is necessary to reduce the resistance and parasitic capacitances of the circuits and controls lines as far as possible. In the case of memories, this can cause a limitation of the number of transistors per line and per column. However, this limitation is significantly compensated by the significant increases in the speed with which the stored charge is removed.

The charge removal process described with reference to Figures 6 and 7 can be enhanced by providing an asymmetrical source/drain junction to give larger junction capacitance on the drain side. In the arrangement described with reference to Figures 1 to 3, it is observed that in order to ensure fast writing of data states represented by the charge level (i.e. in a few nanoseconds), fairly high voltages need to be used, but that these voltages need to be reduced by device optimisation because of reliability problems.

Figure 8 shows a further embodiment of a transistor in which the voltage required to remove charge stored in the body of the transistor is reduced. During discharging of the charged body, pulses are applied to the drain and to the gate of the transistor so that the body/source or body/drain junction is biassed in a forward direction. As a result, the majority carriers are removed from the charged floating body, providing

a decrease in channel current when the transistor is switched to its conductive state (see Figure 4).

The potential of the floating body can be altered by adjusting the voltages applied to the transistor contacts, or by altering the body/source and/or body/drain and/or body/gate capacitances. For example, if the potential of the transistor drain is positive compared to that of the source, the floating body potential can be made more positive by increasing the capacitance between the drain and the floating body. In the arrangement shown in Figure 8, the MOSFET has different doping profiles for the drain and the source. In particular, a P+ doped region is formed in the vicinity of the drain, which leads to an increased capacitance between the drain and the floating body. This is manufactured by adding an implant on the drain side only, and by diffusing this implant before forming the source and drain implanted regions. An alternative is to increase the capacitive coupling between the drain and the floating body by using different geometries for the drain and the source, as shown in Figure 9.

The improved charging and discharging techniques described with reference to figures 5 to 9 enable significantly greater current differences between the uncharged and highest charged states of the transistor to be achieved. For example, in the arrangement disclosed with reference to figures 1 to 3, the current difference between the maximum and minimum charge states is typically 5 to 20μA/μm of device width. For a 0.13 μm technology, where a typical transistor width of 0.2 to 0.3μm would be used, this means that a current difference of about 1 to 6μA is available. At least 1μA of current is required to be

able to sense the data represented by the charged state.

The charging and discharging arrangements disclosed with reference to figures 5 to 9 provide a current difference as high as 110μA/μm. The availability 110μA/μm of signal for devices with 0.2 to 0.3μm width means that current differences of 22 to 33μA per device can be achieved. As 1μA is enough for detection, it can be seen that several levels of charge can be stored in a single transistor body.

It is therefore possible to store multiple bits of data, for example, as shown in Figure 10. Figure 10a shows a simple arrangement in which two levels are available, and one bit of data can be stored. In Figures 10b and 10c, multiple bits of data can be stored in states between the maximum and minimum charging levels. For example, to be able to store two bits of data, a total current window of 3μA is required, while 7μA is required to store three bits per device. With a total window of 33μA, five bits, corresponding to 32 levels, can be stored in the same transistor. It will be appreciated that by storing a data word consisting of several data bits, as opposed to a single data bit, the storage capacity of a semiconductor memory using this technique can be significantly increased.

Figure 11 shows the time dependence of a pulsed charging operation. Charging between different levels can be achieved by creating an initial "0" state, and then repeatedly writing "1" pulses, or by starting from the highest state, and repeatedly writing "0" pulses. One other possibility is to use different writing pulses to obtain different states, for example, by varying the writing pulse amplitude and duration to

obtain a particular level.

A further possibility is shown in figure 12, which shows the levels achievable using the charge pumping principle described with reference to figures 6 and 7. The amount of charge removed after each pulse causes a current decrease of ΔI_s, and the various levels can be obtained by changing the number of charge pumping pulses.

As pointed out above, the charge states of the body of the transistor can be used to create a semiconductor memory device, data "high" states being represented by a positive charge on body 20, and data "low" states being represented by a negative or zero charge. The data stored in the transistor can be read out from the memory device by comparing the source-drain current of the transistor with that of an uncharged reference transistor.

A DRAM (dynamic random access memory) device operating according to this principle is shown in Figure 13. A DRAM device is formed from a matrix of data storage cells, each cell consisting of a field effect transistor of the type shown in Figure 1, 5, 6, 7, 8 or 9, the sources of the transistors of each row being connected together, and the gates and drains of the transistors of each column being connected together, a transistor 32_{ij} corresponding to a transistor located on column I and row j,the transistor 32_{22}being highlighted in Figure 13 The gate 28, source 18 and drain 22 of transistor 32_{ij} are connected to conductive tracks 40i 42i and 44j respectively. The conductive tracks 40, 42 and 44 are connected to a control unit 46 and a reading unit 48, the construction and operation

of which will be familiar to persons skilled in the art. The sources are earthed via the reading unit 48, or may be connected to a given fixed potential.

The operation of the memory device shown in Figure 13 will now be described.

Initially, all gates (tracks 40) are at -2V, and all drains (tracks 44) and sources (tracks 42) are held at 0V. In order to write a data bit of state ''1'' to a transistor 32_{ij}, all tracks 40 of columns different from i are still held at -2V, while track 40i is brought to -1.5V. During the time that the potential of track 40i is -1.5V, all tracks 44 of rows different from j are still held at 0V, while the potential of track 44j is brought to -2V. This process generates a positive charge in the body of transistor 32_{ij}, as described above with reference to Figure 2, the positive charge representing a single data bit of state "1". The potential of track 44j is then brought back to 0V, and the potential of track 40i is subsequently brought back to -2V.

In order to write a data bit of state "zero" to the transistor 32_{ij}, from the condition in which all gates are initially held at -2V and all sources and drains are held at 0V, track 40i is brought to a voltage of +1V, the other tracks 40 being held at -2V. During the time that the potential of track 40i is +1V, all tracks 44 of rows other than j are held at 0V, while the potential of track 44j is brought to -2V. This generates a net negative charge in the body of the transistor and the potential of track 44j is then brought back to 0V. The potential of track 40i is then subsequently brought back to -2V.

In order to read the information out of the transistor 32_{ij} the voltage of tracks 40 of columns different from i is brought to 0V, while track 40i is held at 1V, and the voltage of tracks 44 of rows different from j is brought to 0V, while track 44j is held at +0.3V. As shown in Figure 13, this then enables the current on track 44j, which is representative of the charge in the body of transistor 32_{ij}, to be determined. However, by applying a drain voltage of 0.3V, this also provides the advantage that unlike conventional DRAM devices, the reading of data from transistor 32_{ij} does not discharge the transistor 32_{ij}. In other words ,because the step of reading data from the data storage cell does not destroy the data stored in the cell, the data does not need to be refreshed (i.e. rewritten to the transistor 32_{ij}) as frequently as in the prior art.

However, it will be appreciated by persons skilled in the art that the electric charge stored in the body of transistor 32_{ij} decays with time as a result of the electric charges migrating and recombining with charges of opposite sign, the time dependence of which depends on a number of factors, including the temperature of the device, or the presence of radiation or particles such as photons striking the transistor. A further application of this will be described in more detail below.

In the memory unit described with reference to Figure 13, each data storage cell is formed by a transistor 32 disposed in an insulating honeycomb structure 24. The source and drain of neighbouring transistors are located adjacent the drain and source of the two neighbouring transistors in the same row, respectively. A DRAM device of a second embodiment is shown in

Figure 14, in which parts common to the embodiment of Figure 13 are denoted by like reference numerals. In the embodiment of Figure 14, for each row of transistors, other than those arranged at the ends, each transistor shares its drain and source region with its neighbours. This enables the number of tracks 42 and connections on tracks 44 to be reduced almost by a factor of 2.

A cross-sectional view of the DRAM device of Figures 14 and 15 is shown in Figure 16, the view being taken along the line A-A in Figure 15. The device comprises a substrate 13 including a silicon wafer 10 and insulating layer 12 as in Figure 1, with sources 18, bodies 20 and drains 22 being formed on the insulating layer 12. Dielectric films 26 are provided on bodies 20, and are extended upwards to the side of gates 28. The gates are interconnected by tracks 40 and the sources 18 are interconnected via respective pillars 50 by tracks 42, the tracks 40, 42 extending parallel to each other in a direction perpendicular to the plane of the paper of Figure 16. The drains 22 are interconnected via respective pillars 52 by tracks 44 extending in a direction perpendicular to tracks 40, 42, and of which only one is shown in Figure 16.

As will be familiar to persons skilled in the art, in order to periodically refresh the data contained in the cells of the memory device, alternate reading and writing operations can be carried out, with part of the charge detected during reading being supplemented in the transistor in question. The refreshing frequency typically ranges from 1 ms to 1 second, a more detailed description of which is provided in ADRAM circuit design ISBN0-78036014-1.

As well as using charging of the body of a transistor as described above to construct a DRAM memory device, the charging process can be applied to other types of memory, such as SRAM (static random access memory). One particular application is to cache SRAM applications. In modern microprocessors (MPU), the DRAM/MPU performance gap illustrated in Figure 17 has forced the MPU manufacturers to add some memory to the MPU. This memory is called cache memory. For example, the Intel 486 processor used 8Kbytes of cache memory. This memory is used to store information that is needed frequently by the MPU. In modern Pentium processors, a second level of cache memory, up to 256 Kbytes, has been added to keep up performance. According to industry trends, next generation processors (the 10 Ghz Pentium processors for example) will require a third level of cache memory having a density of 8 to 32 Mbytes of cache.

This memory has previously been provided by a 6 transistor SRAM cell (6T). The cell occupies typically an area of 100 to 150 F^2, where F is the minimum feature size, which is quite large. Applying the charge storing concept set out above, a 1T (1 transistor) cell can replace the 6T transistor cell. Integrated in a logic technology, it can occupy a 10 to 15 F^2 area, which is 10 times less. This is of significant importance since integrating tens of Mbytes of 6T SRAM cells required die sizes much too large for practical fabrication.

As pointed out above, the charge stored on the body of a transistor can also represent some physical parameter to be measured, for example the incidence of optical radiation. Figure 18 is a schematic representation of a CMOS image sensor

embodying the present invention.

Image sensors have hitherto been made with a matrix of photosensitive devices, each of which is provided with a MOS transistor acting as a switch. To boost the information contained in each pixel, the pixel itself is also provided with an in-built amplifier. Such pixels are called active pixel sensors (APS) and typically include several devices: photo gate APS have typically 1 photosensitive capacitor and 4 transistors. Photodiode APS have typically 1 photosensitive diode and 3 or 4 transistors. In these APS devices the incoming light is incident on the circuit (sometimes through a lens) and hits the sensitive element of the device. An integration cycle then allows charge generated by the incoming optical radiation to be accumulated and to generate an electrical signal in a few ms or a few tens of ms. This signal is then amplified and read. The matrix organization is similar to a memory matrix organization, a typical pixel size being about 400 F^2, where F is the technology minimum feature size.

In the arrangement shown in Figure 18, it is possible to create a full pixel with a single transistor that acts at the same time as light sensitive element and as an amplifier. To achieve this, SOI transistors are arranged in a matrix arrangement similar to that described for the DRAM applications above. The incoming light can come from the top or from the bottom (in this second case, an advantageous feature of SOI technology being that the silicon substrate below the buried oxide can be removed locally in the sensor matrix to provide an easy rear side illumination option).

To operate the sensor, a reset operation is required, the reset operation consisting of removing the majority carriers from the floating body (holes in the case of an NMOS transistor). For an NMOS device this means putting all devices in what is called a A0@ state in the DRAM application. That this reset operation can be achieved by hole evacuation as described with reference to Figures 1 to 3, or more preferably by the charge pumping technique described with reference to Figures 6 and 7. When the reset has been carried out (in typically 1 μs), the light then creates electron hole pairs in the body of the device. The minority carriers are removed through the junction and the majority carriers accumulate in the body, allowing the charge integration. The information is read like in a DRAM memory, as explained above. The pixel area achievable with such devices can be as small as $4F^2$, or 100 times smaller than in prior art devices. These imagers can be used in various applications, such as portable video recorders, digital photography, web cams, PC cameras, mobile telephones, fingerprint identification, and so on.

It will be appreciated by persons skilled in the art that the above embodiments have been described by way of example only and not in any limitative sense, and that various alterations and modifications are possible without departure from the scope of the invention as defined by the appended claims. For example the process, described with reference to NMOS transistors, can also be applied to PMOS transistors, in which case the stored charge is negative, i.e., formed by electrons, and that the free particles in the channel are holes. In that case, the channel is produced by the application of a negative potential to the gate. Also, in certain types of SOI transistors, the

substrate can also act as a gate. In that case, the insulating layer performs the function of the dielectric film and the channel is formed at the interface of the body and the insulating layer. In addition, the invention can be applied to JFET (junction field effect transistor) technology as well as to the MOSFET technology described above. Furthermore, instead of providing a layer of insulating material on the silicon substrate, adjacent transistors can be electrically isolated from each other by means of a layer of n-type silicon on the silicon substrate, and biassing the n-type silicon layer such that the junction formed by the p-type transistor body and the n-type silicon is reverse biassed. In such cases, the body region of each transistor should also extend below the corresponding source and drain regions to separate the source and drain regions from the n-type silicon layer, and adjacent transistors are isolated from each other by means of a silicon dioxide layer extending downwards as far as the n-type silicon layer.

CLAIMS

1. A semiconductor device comprising :-

a substrate;

at least one data storage cell provided on one side of said substrate, wherein the or each said data storage cell comprises a respective field effect transistor comprising (i) a source; (ii) a drain; (iii) a body arranged between said source and said drain and adapted to at least temporarily retain a net electrical charge generated in said body such that the magnitude of said net charge can be adjusted by input signals applied to said transistor; and (iv) at least one gate adjacent said body; and

charge adjusting means for at least partially cancelling the adjustment of said net electrical charge by said input signals, by applying first predetermined electrical voltage signals between at least one corresponding said gate and the corresponding said drain and between the corresponding said source and said drain.

2. A device according to claim 1, wherein said input signals comprise second predetermined electrical voltage signals

applied between at least one corresponding said gate and the corresponding said drain and between the corresponding said source and said drain.

3. A device according to claim 2, wherein the device is a memory device.

4. A device according to any one of the preceding claims, wherein the device is a sensor and the charge stored in at least one said body in use represents a physical parameter.

5. A device according to any one of the preceding claims, wherein said input signals comprise electromagnetic radiation.

6. A device according to claim 5, wherein the device is an electromagnetic radiation sensor.

7. A device according to any one of the preceding claims, further comprising a first insulating layer at least partially covering said substrate, wherein the or each said data storage cell is provided on a side of said first insulating layer remote from said substrate.

8. A device according to claim 7, wherein said first insulating

layer comprises a layer of semiconductor material of opposite doping type to the body of the or each said data storage cell.

9. A device according to any one of the preceding claims, further comprising a respective second insulating layer provided between at least one said body and the or each corresponding said gate.

10. A device according to claim 9, wherein at least one said transistor includes a plurality of defects in the vicinity of the interface between at least one corresponding said body and the corresponding said second insulating layer, for trapping charge carriers of opposite polarity to the charge carriers stored in the body.

11. A device according to claim 10, wherein the density of defects in the vicinity of said interface is between 10^9 and 10^{12} per cm^2.

12. A device according to any one of the preceding claims, further comprising data reading means for causing an electrical current to flow between a said source and a said drain of at least one said data storage cell by applying third predetermined electrical voltage signals between at least one

corresponding said gate and said drain and between said source and said drain.

13. A device according to any one of the preceding claims, wherein said first insulating layer comprises a plurality of insulating layers.

14. A device according to any one of the preceding claims, wherein at least one said data storage cell is adapted to store at least two distinguishable levels of said electrical charge.

15. A device according to claim 14, wherein at least one said data storage cell is adapted to store at least three distinguishable levels of said electrical charge.

16. A device according to any one of the preceding claims, wherein at least one said transistor has a drain/body capacitance greater than the corresponding source/body capacitance.

17. A device according to claim 16, wherein the body of at least one said transistor has a higher dopant density in the vicinity of said drain than in the vicinity of said source.

corresponding said gate and said drain and between said source and said drain.

13. A device according to any one of the preceding claims, wherein said first insulating layer comprises a plurality of insulating layers.

14. A device according to any one of the preceding claims, wherein at least one said data storage cell is adapted to store at least two distinguishable levels of said electrical charge.

15. A device according to claim 14, wherein at least one said data storage cell is adapted to store at least three distinguishable levels of said electrical charge.

16. A device according to any one of the preceding claims, wherein at least one said transistor has a drain/body capacitance greater than the corresponding source/body capacitance.

17. A device according to claim 16, wherein the body of at least one said transistor has a higher dopant density in the vicinity of said drain than in the vicinity of said source.

18. A device according to claim 16 or 17, wherein the area of the interface between the drain and body of at least one said transistor is larger than the area of the interface between the source and the body.

19. A device according to any one of the preceding claims, wherein common source and/or drain regions are shared between adjacent transistors of said device.

20. A method of storing data in a semiconductor device comprising a substrate, and at least one data storage cell provided on one side of said substrate, wherein the or each said data storage cell comprises a respective field effect transistor comprising (i) a source; (ii) a drain; (iii) a body arranged between said source and said drain and adapted to at least temporarily retain a net electrical charge generated in said body such that the magnitude of said net charge can be adjusted by input signals applied to said transistor; and (iv) at least one gate adjacent said body; the method comprising the steps of:

applying first predetermined electrical voltage signals between at least one corresponding said gate and the corresponding said drain and between the corresponding said source and said drain

to at least partially cancel the adjustment of said net charge by said input signals.

21. A method according to claim 20, further comprising the step of applying second predetermined electrical voltage signals between at least one said gate of a said data storage cell and the corresponding said drain and between the corresponding said source and said drain.

22. A method according to claim 21, wherein the step of applying second predetermined said electrical signals adjusts the charge retained in the corresponding said body by means of the tunnel effect.

23. A method according to claim 22, wherein the charge is adjusted by the application of a voltage signal between at least one said gate and the corresponding drain such that at the interface between the corresponding body and the drain, the valence and conduction bands of the body and drain are deformed to inject electrons from the valence band to the conduction band by the tunnel effect, causing the formation of majority carriers in the body.

24. A method according to claim 22 or 23, wherein said charge

is adjusted by means of tunnelling of electrons from the valence band to at least one gate of a said field effect transistor.

25. A method according to any one of claims 20 to 24, wherein the step of applying first predetermined said voltage signals comprises applying electrical voltage signals between at least one said gate and the corresponding said drain such that at least some of the charge carriers stored in the corresponding body recombine with charge carriers of opposite polarity in said body.

26. A method according to claim 25, further comprising the step of applying at least one said voltage signal comprising a first part which causes a conducting channel to be formed between the source and the drain, the channel containing charge carriers of opposite polarity to the charge carriers stored in said body, and a second part which inhibits formation of the channel, and causes at least some of said stored charge carriers to migrate towards the position previously occupied by said channel and recombine with charge carriers of opposite polarity previously in said channel.

27. A method according to claim 26, further comprising the step

of repeating the step of applying at least one said voltage signal in a single charge adjustment operation sufficiently rapidly to cause at least some of said charge carriers stored in the body to recombine with charge carriers of opposite polarity before said charge carriers of opposite polarity can completely migrate to said source or said drain.

Fig. 1

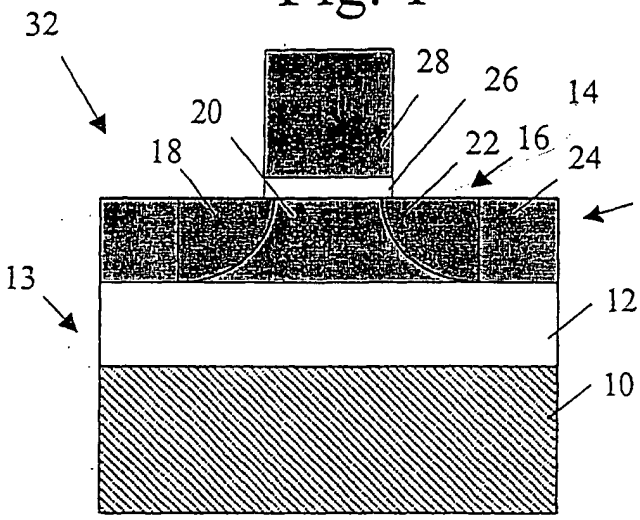


Fig. 2

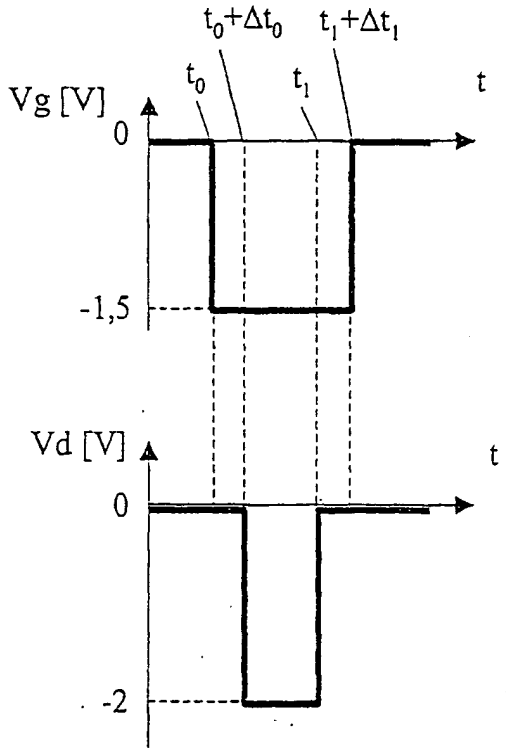
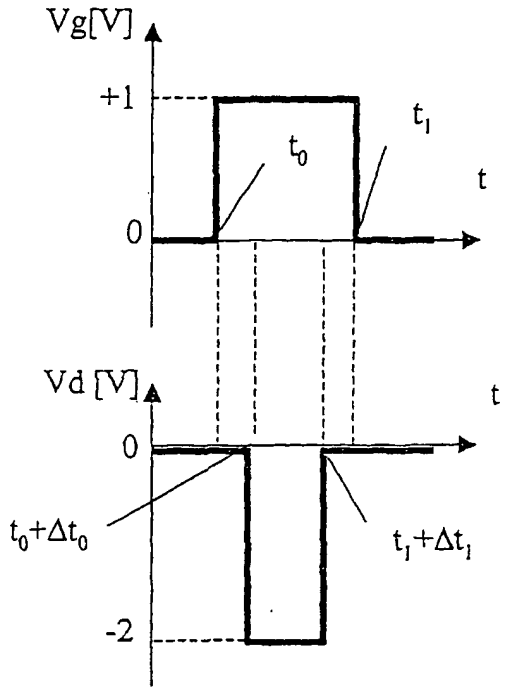


Fig. 3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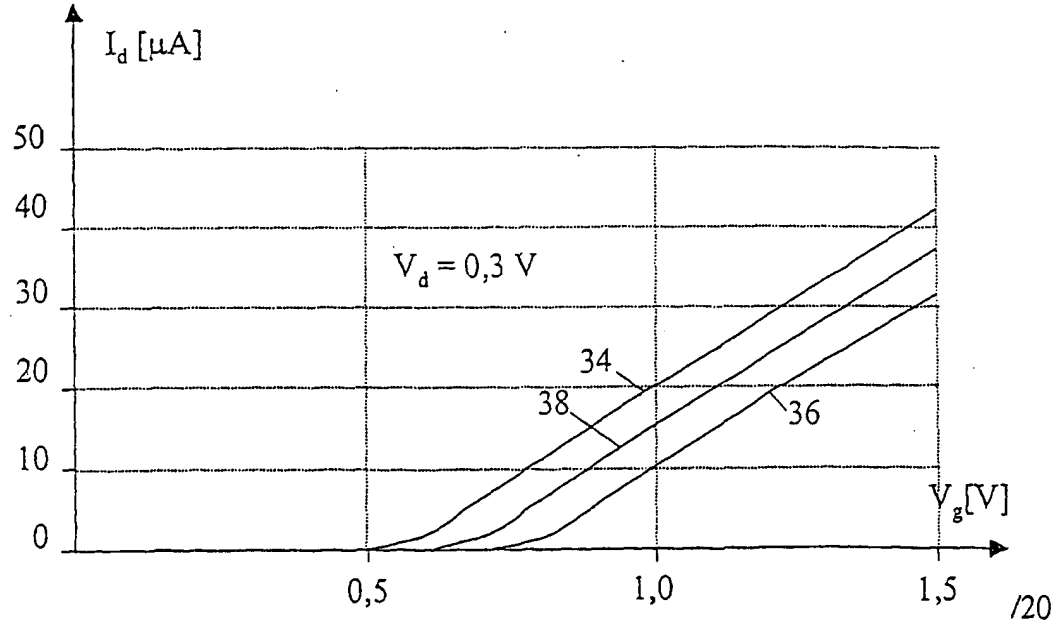
t_0
t_1
t
Vd [V]
0
-2
$t_0+\Delta t_0$
$t_1+\Delta t_1$
t

Fig. 4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40
30
20
10
0
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34
38
36
V_g[V]
0,5
1,0
1,5

Fig. 5a

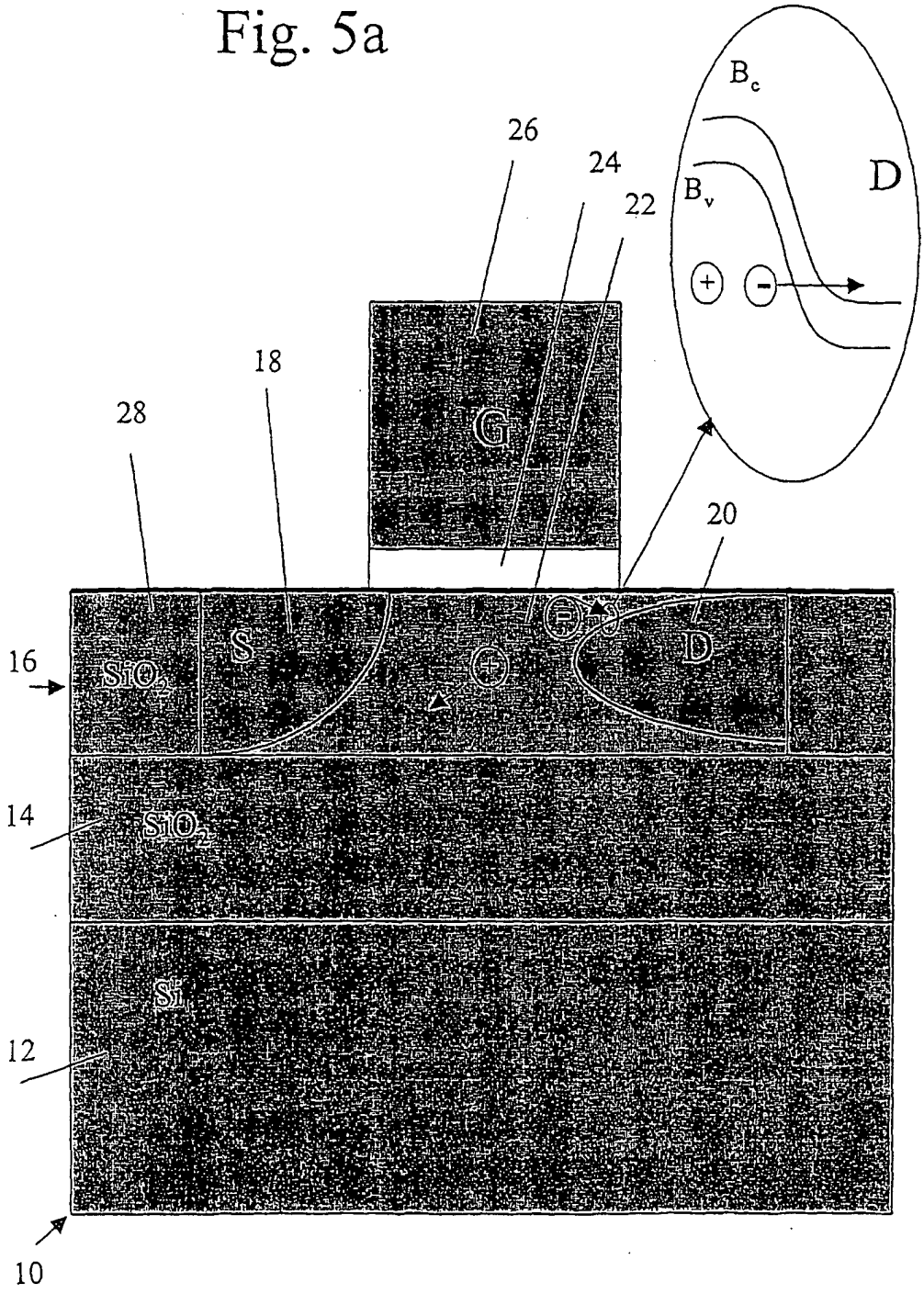


Fig. 5b

Fig. 6a

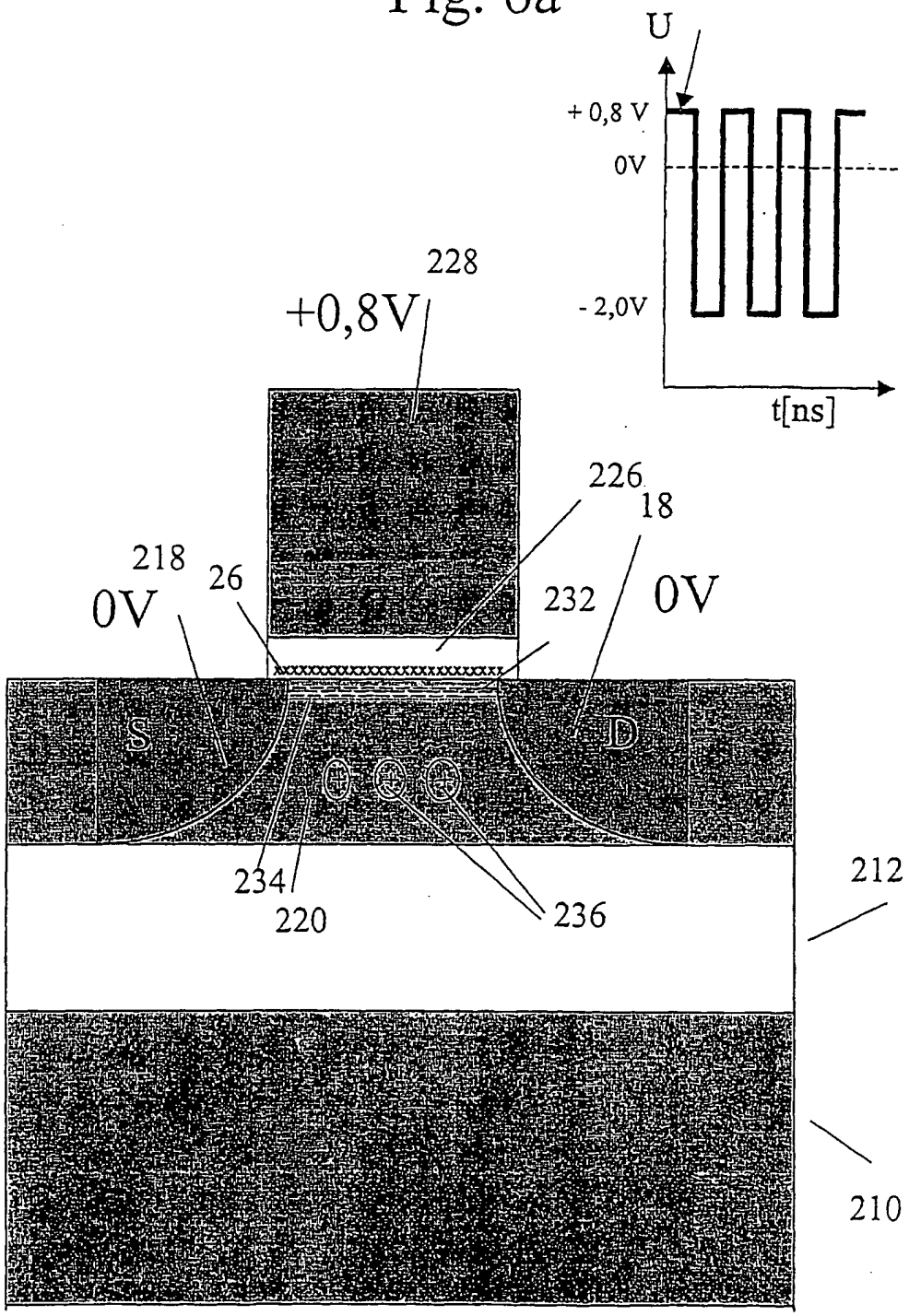


Fig. 6b

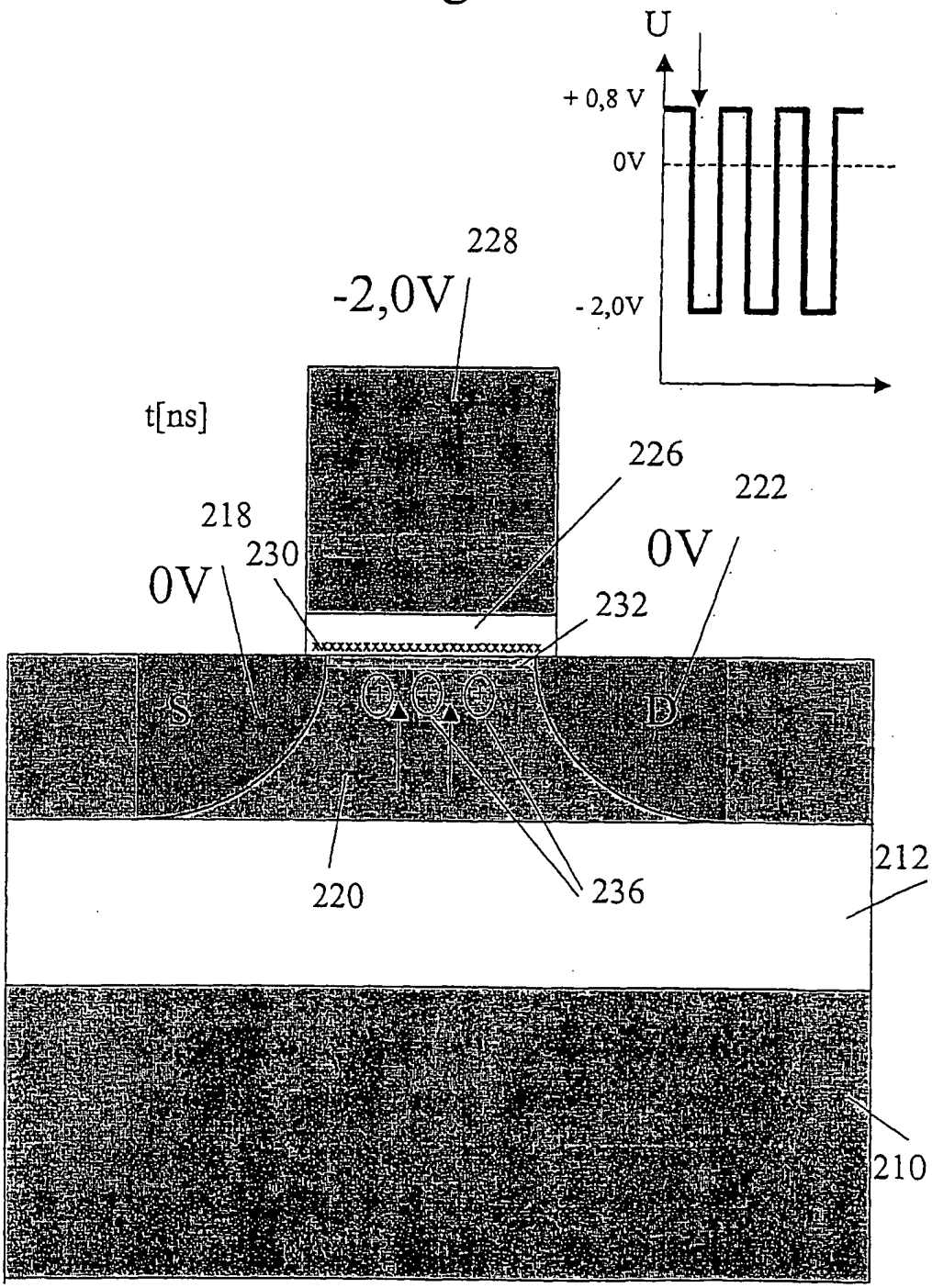


Fig. 6c

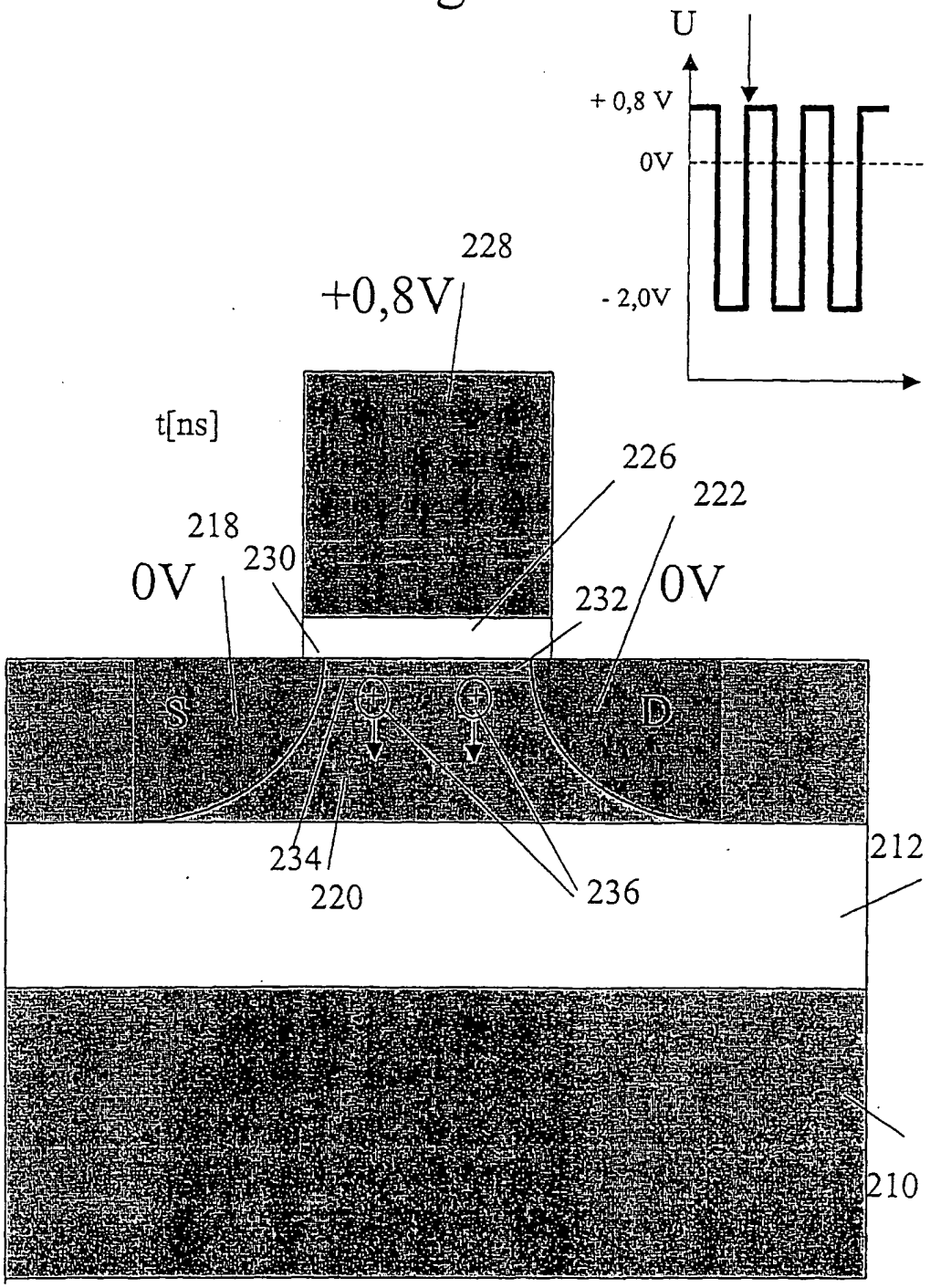


Fig. 7a

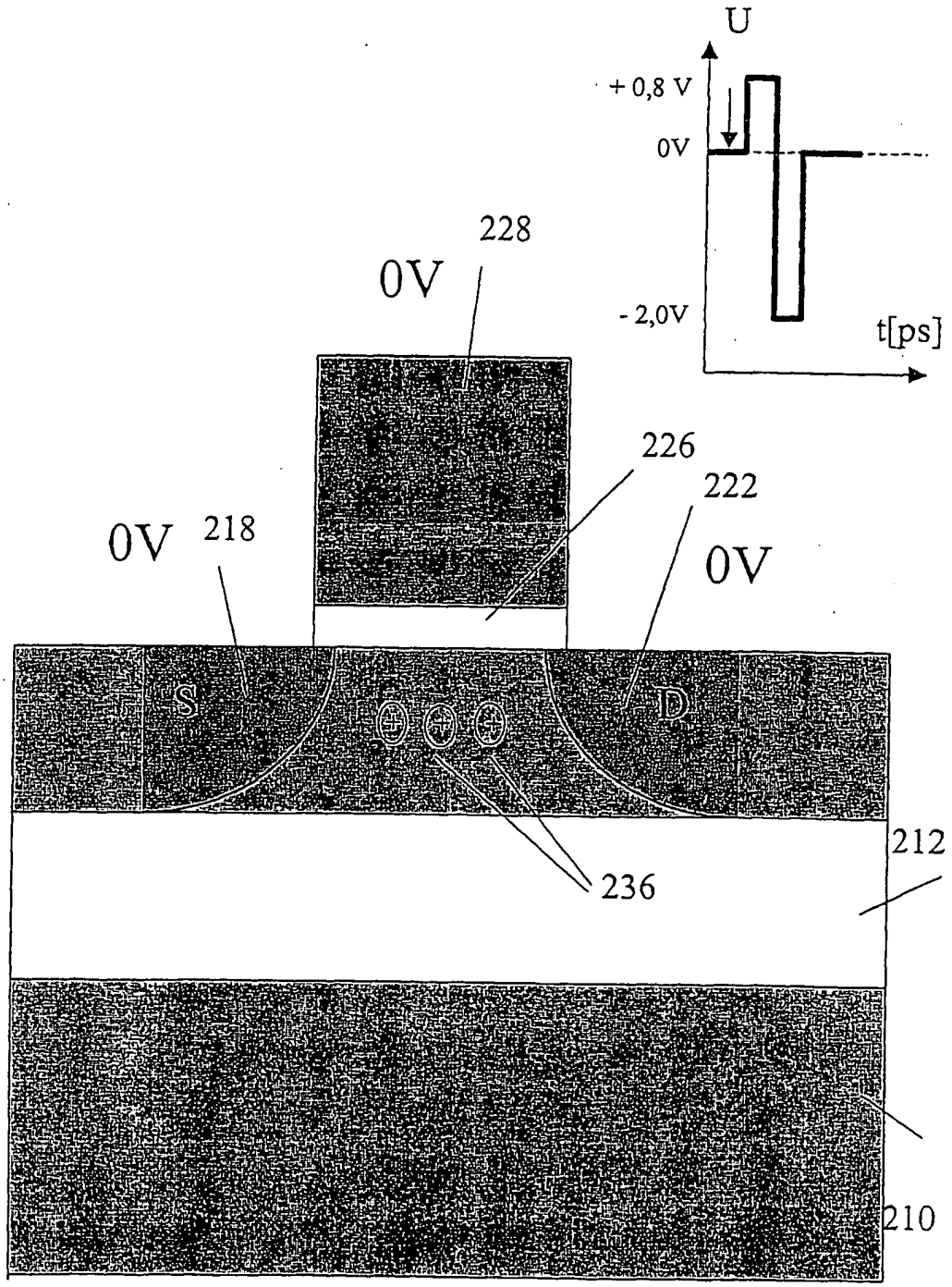


Fig. 7b

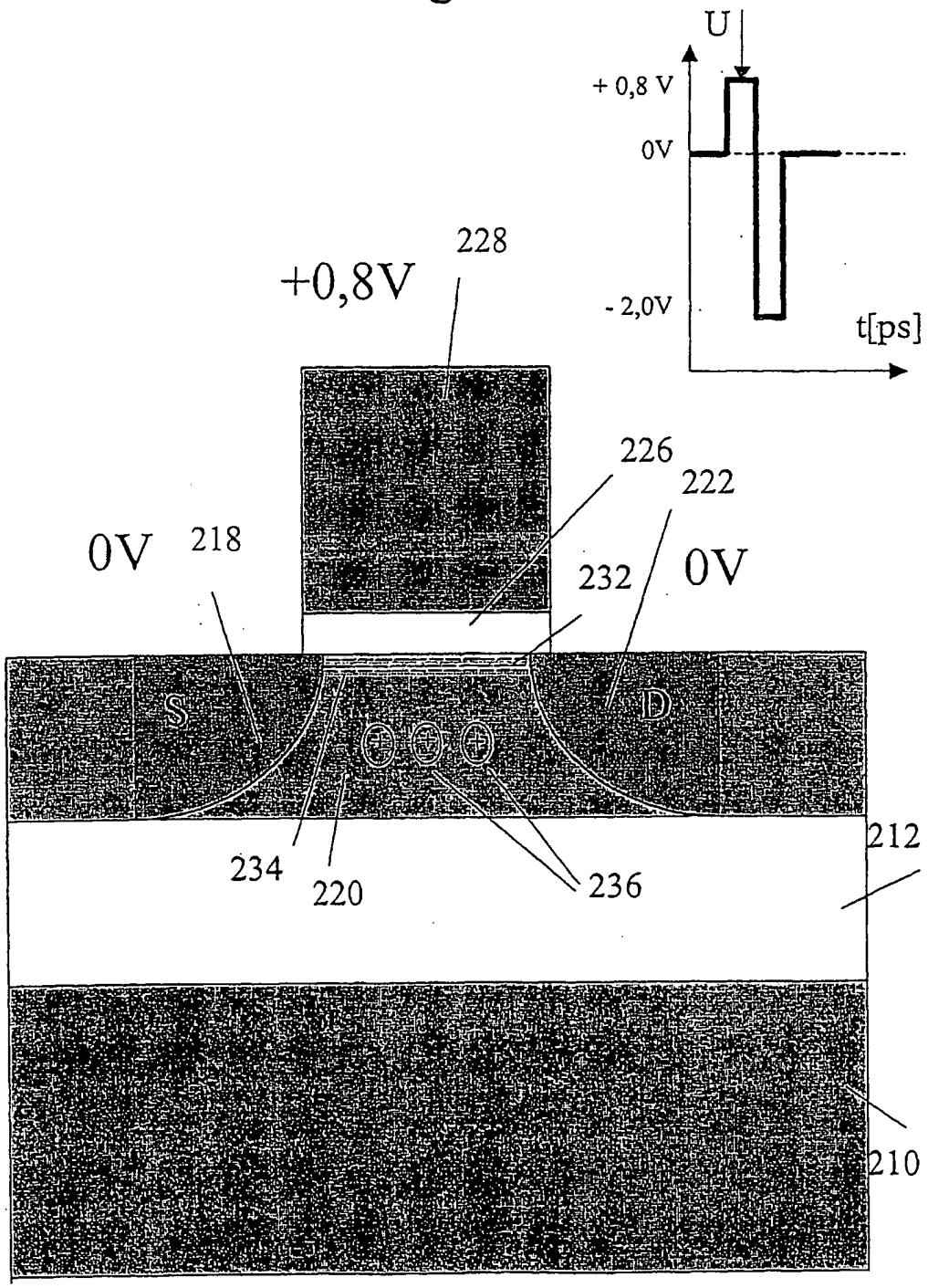


Fig. 7c

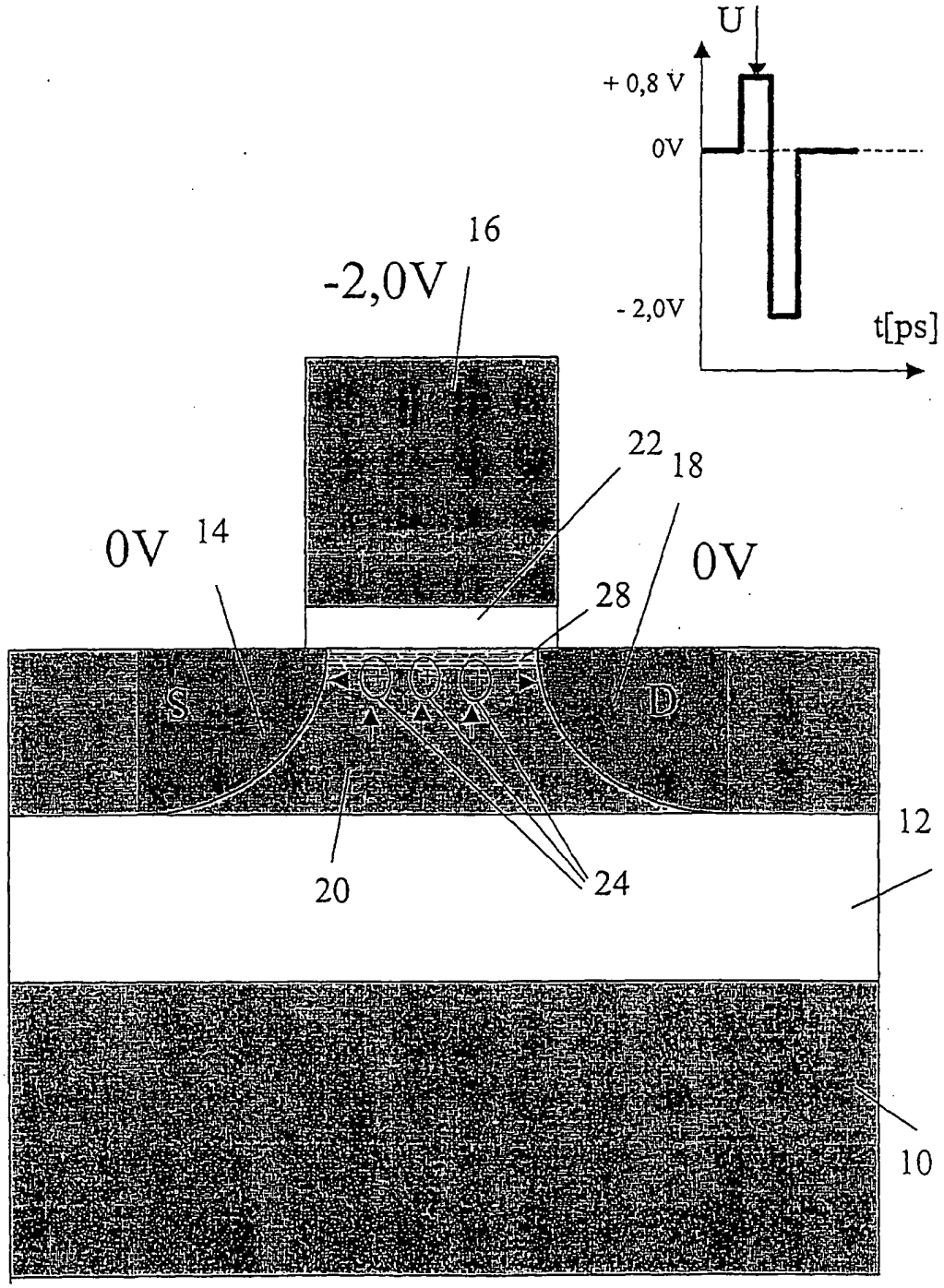


Fig. 7d

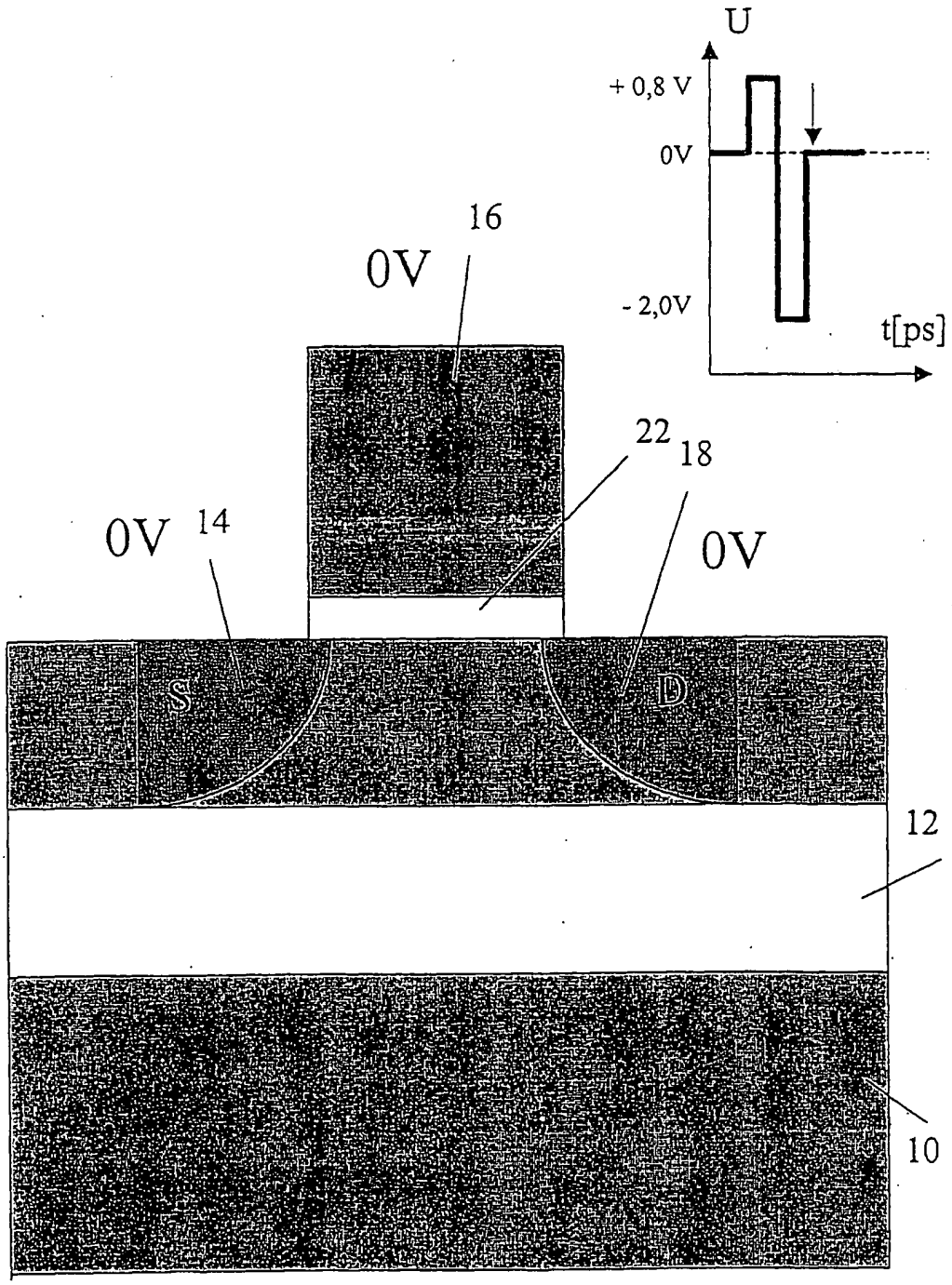


Fig. 8

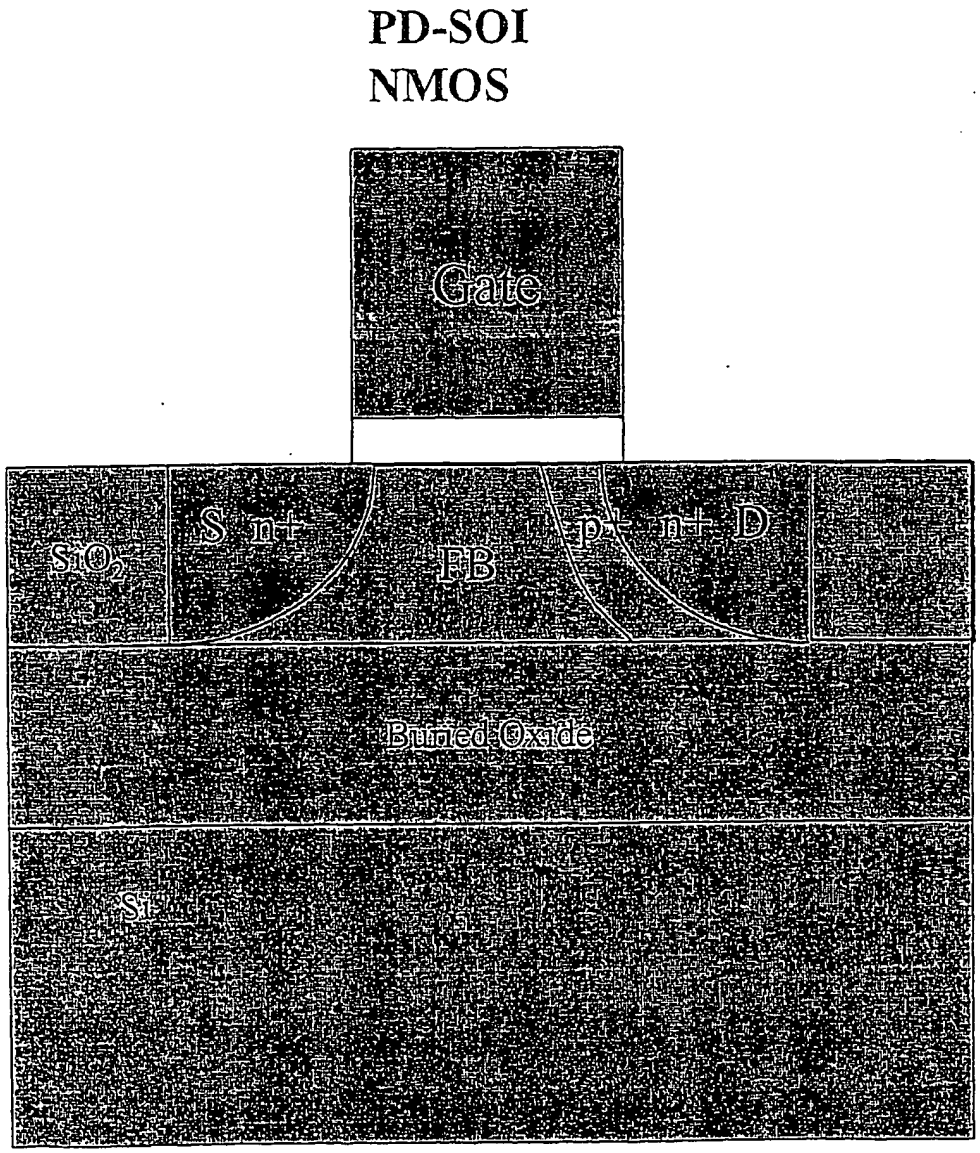


Fig. 9

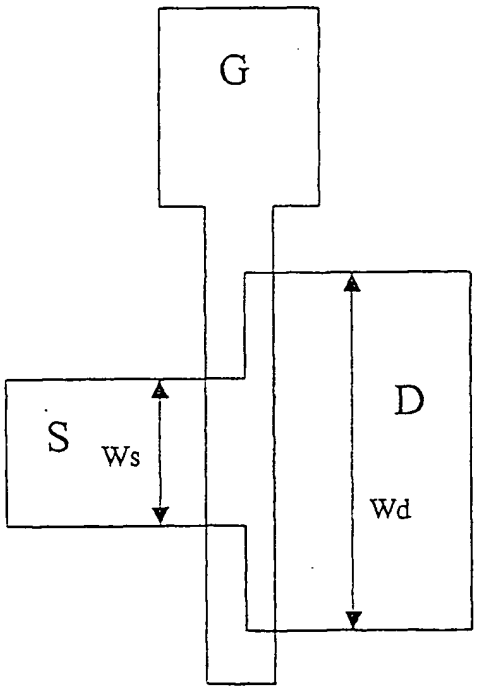


Fig. 10

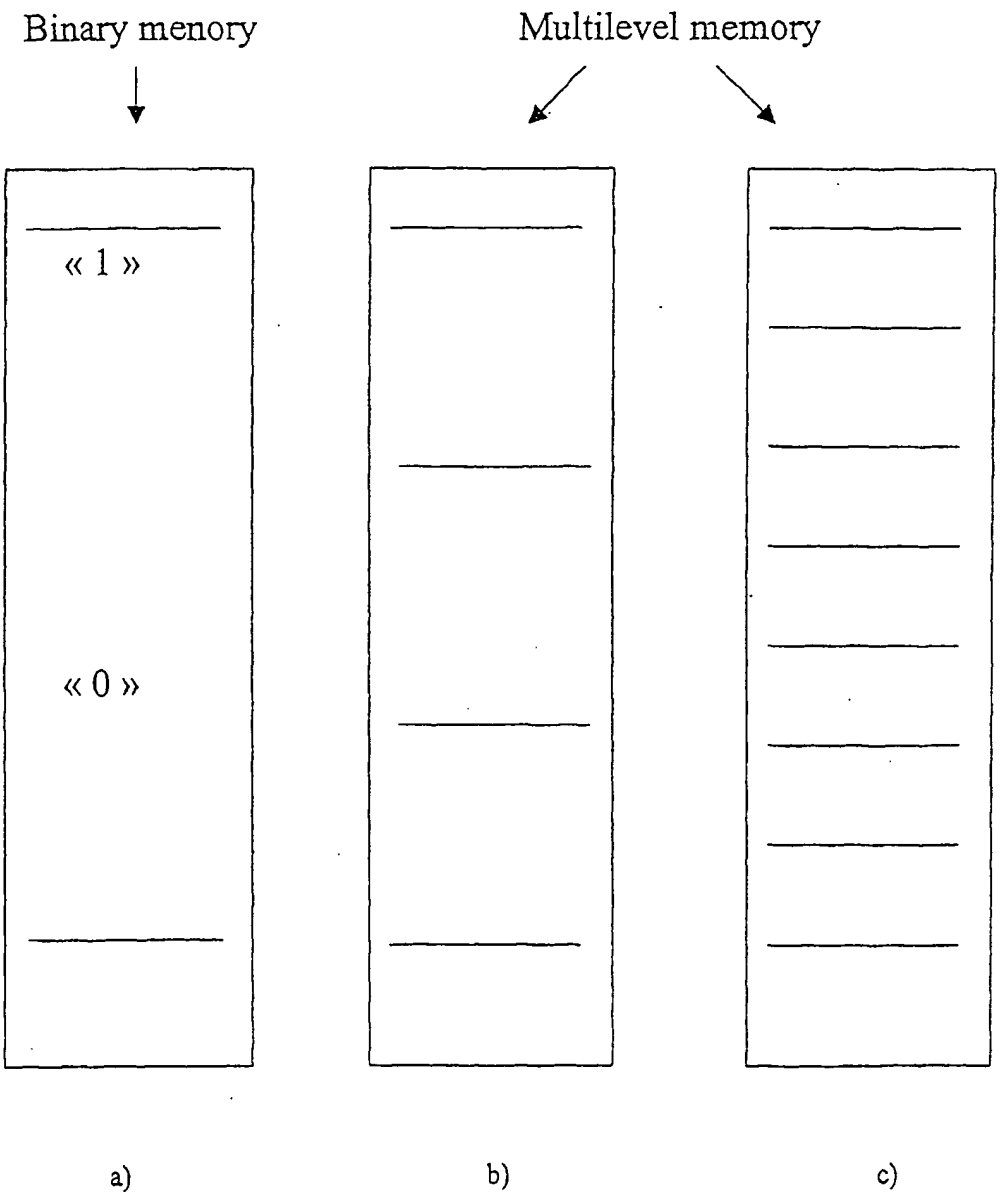


Fig. 11

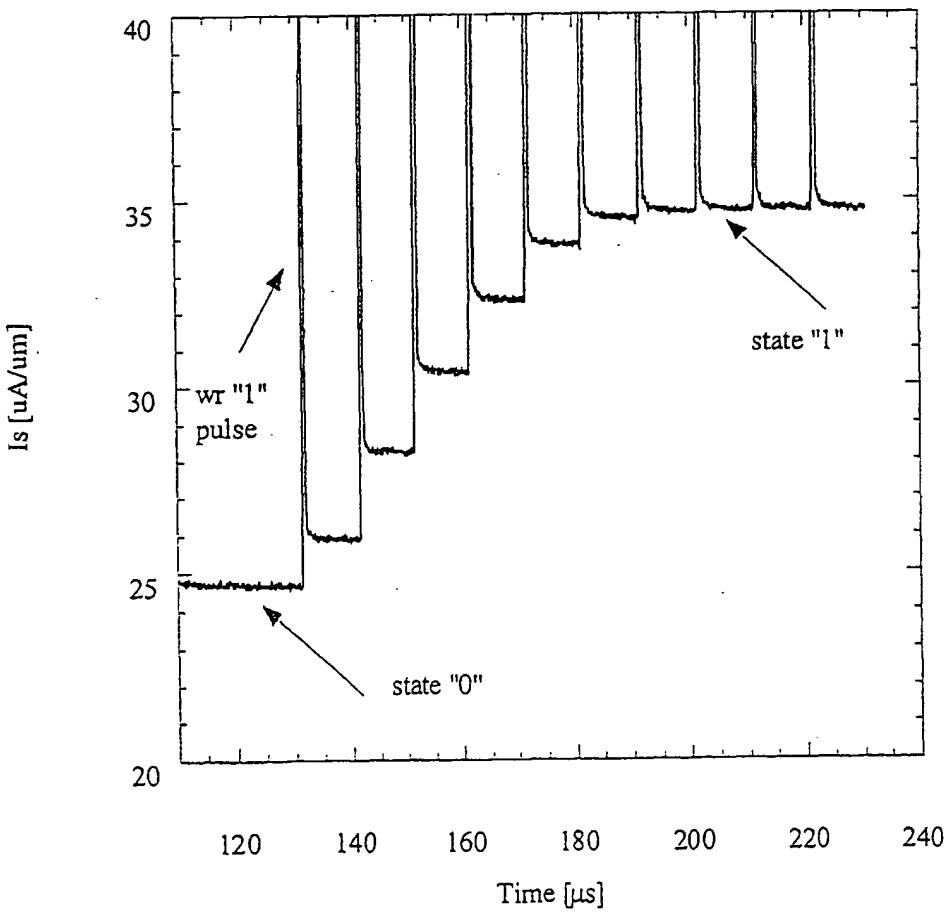
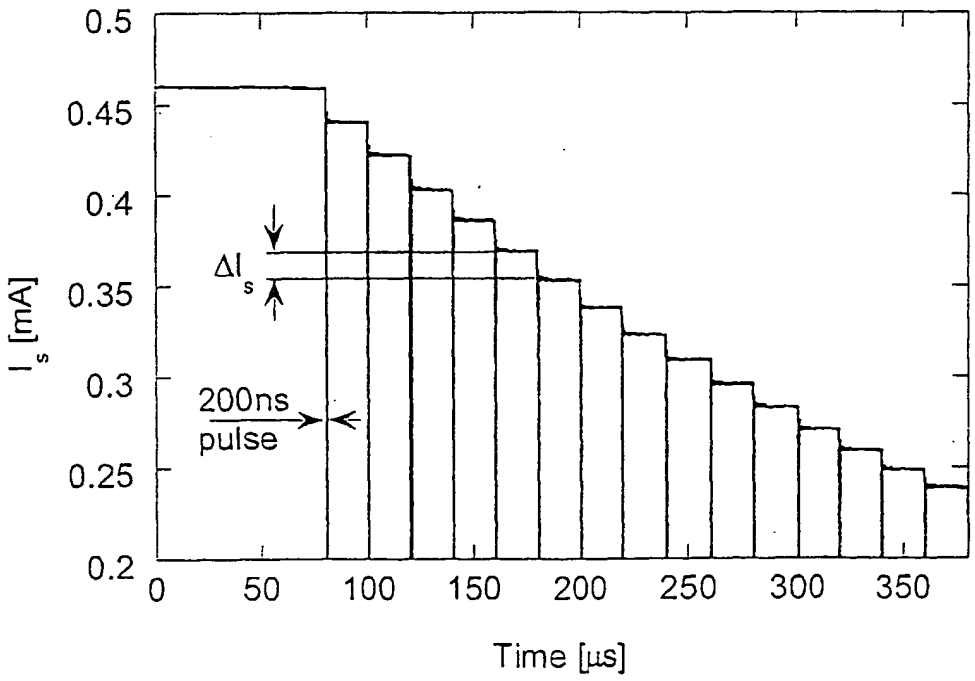

40
35
30
25
20
Is [uA/um]
wr "1"
pulse
state "1"
state "0"
120
140
160
180
200
220
240
Time [µs]

Fig. 12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0.4
0.35
0.3
0.25
0.2
I_s [mA]
ΔI_s
200ns
pulse
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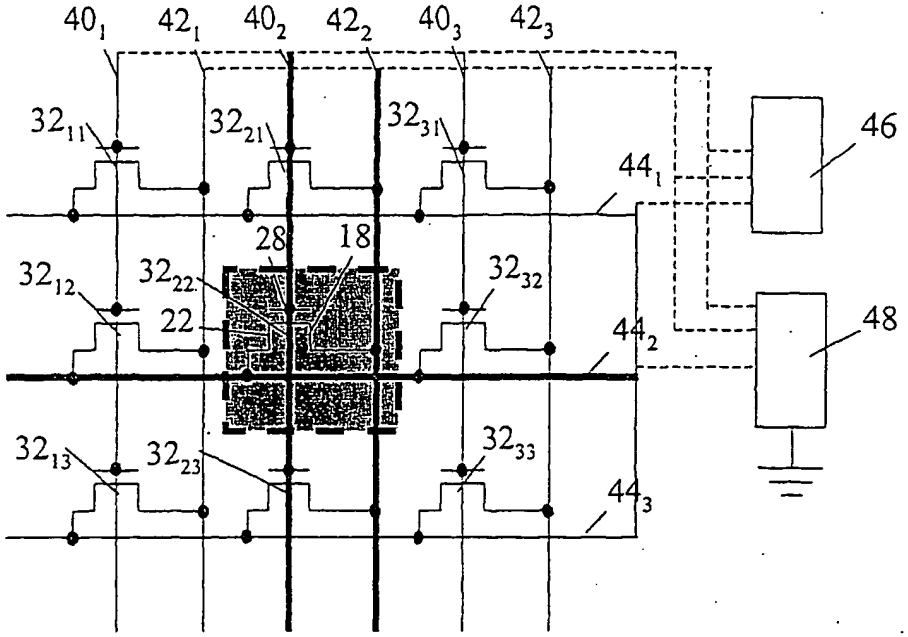
50
100
150
200
250
300
350
Time [µs]

Fig. 13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32₂₁
32₃₁
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18
32₁₂
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32₃₂
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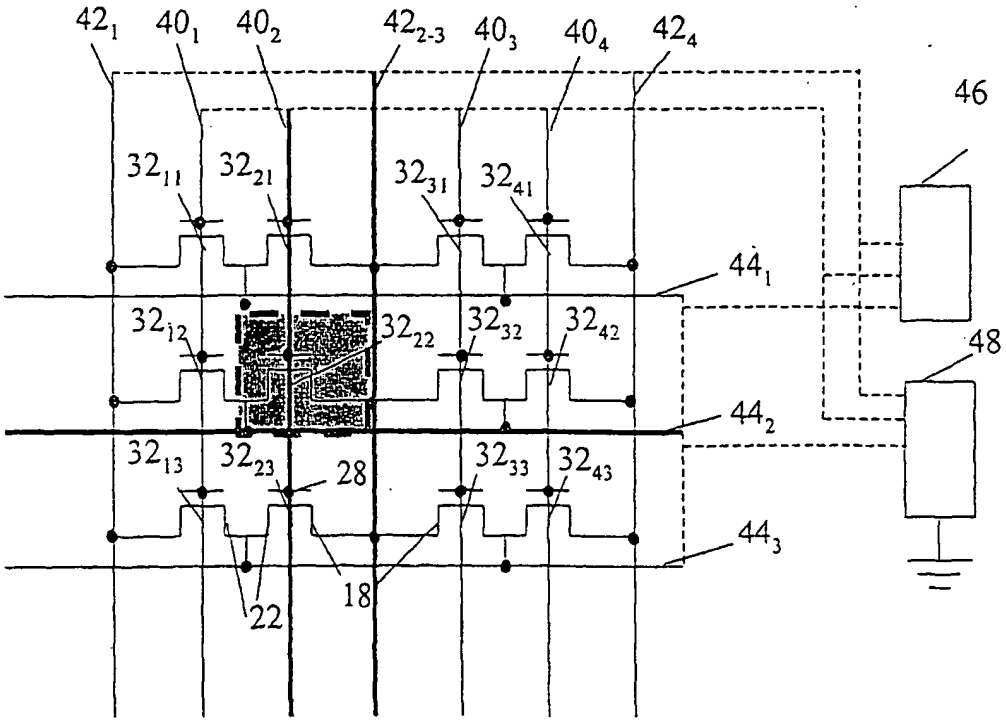
48
44₂
32₁₃
32₂₃
32₃₃
44₃

Fig. 14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44₁
32₁₂
32₂₂
32₃₂
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32₃₃
32₄₃
44₃
22
18

Fig. 15

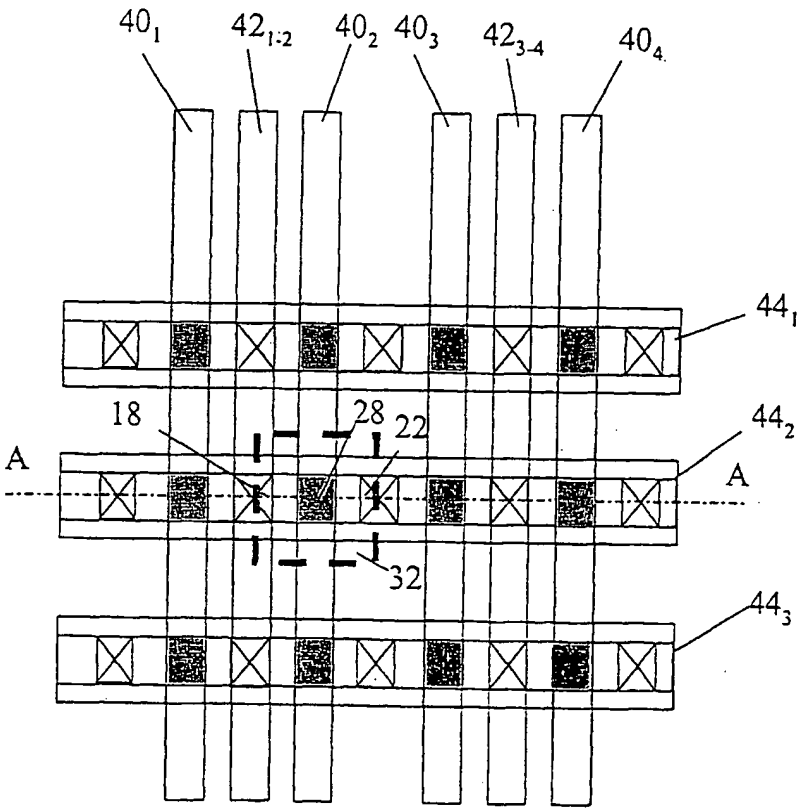

Fig. 16

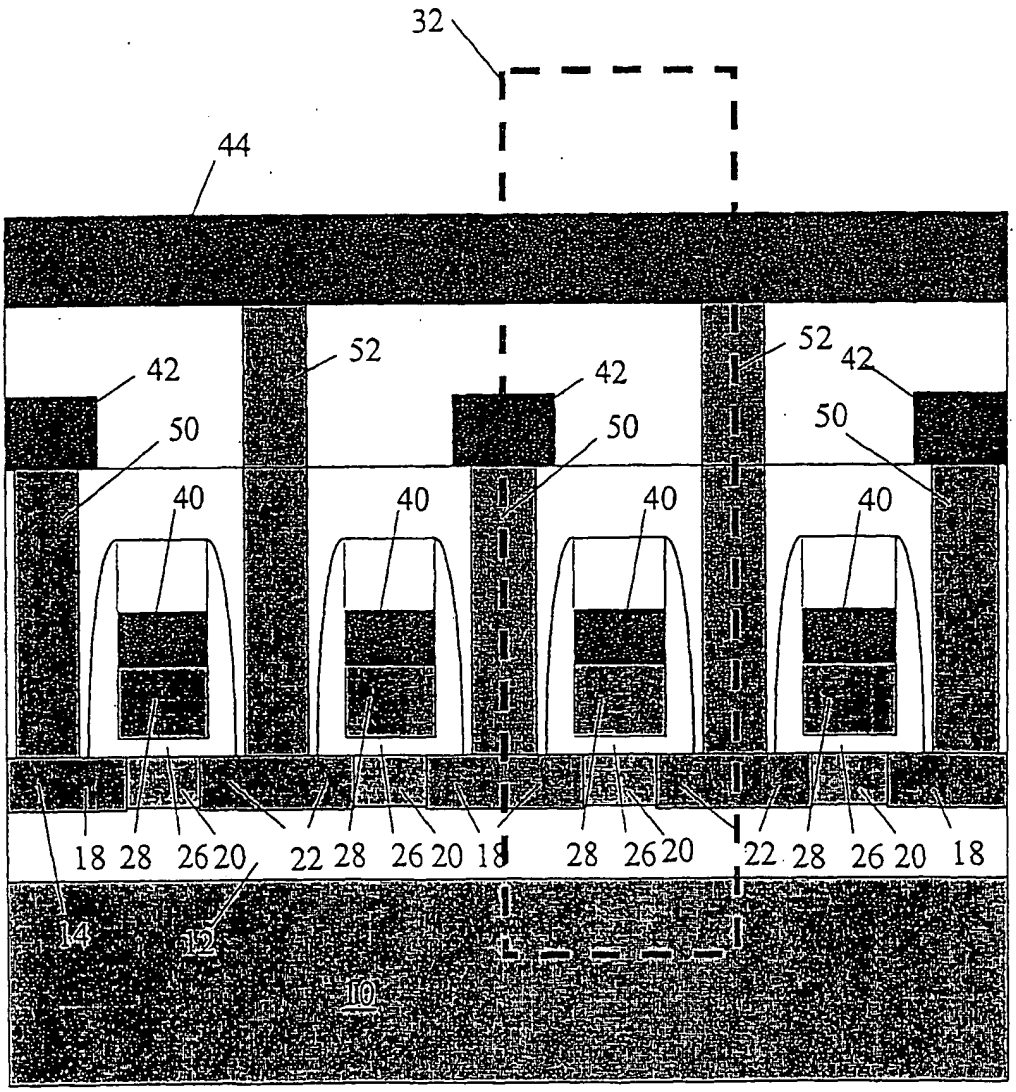

Fig. 17

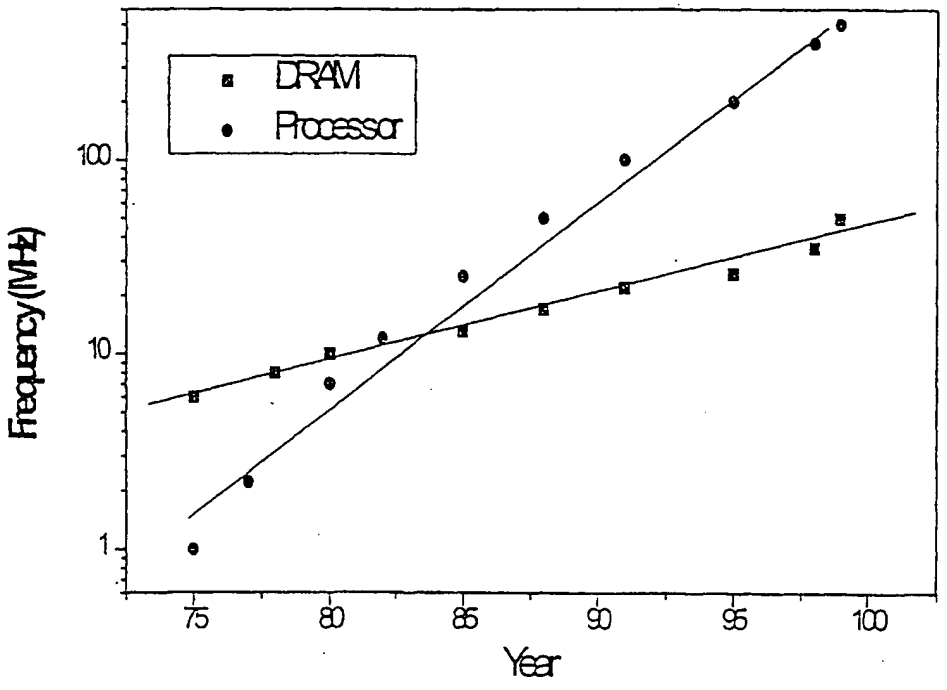

Fig. 18

Shematic of a sensor array